

59A, 100V N-CHANNEL MOSFET

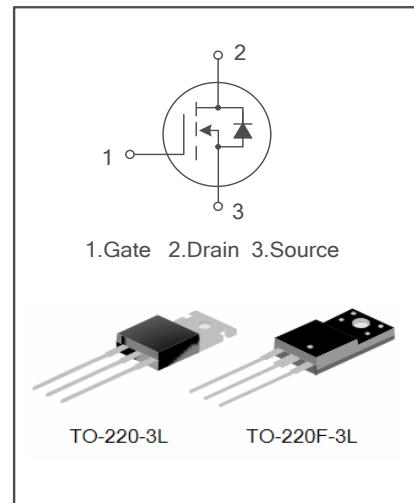
GENERAL DESCRIPTION

SFP59N10 is an N-channel enhancement mode power MOS field effect transistor which is produced using Hi-semicon's proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

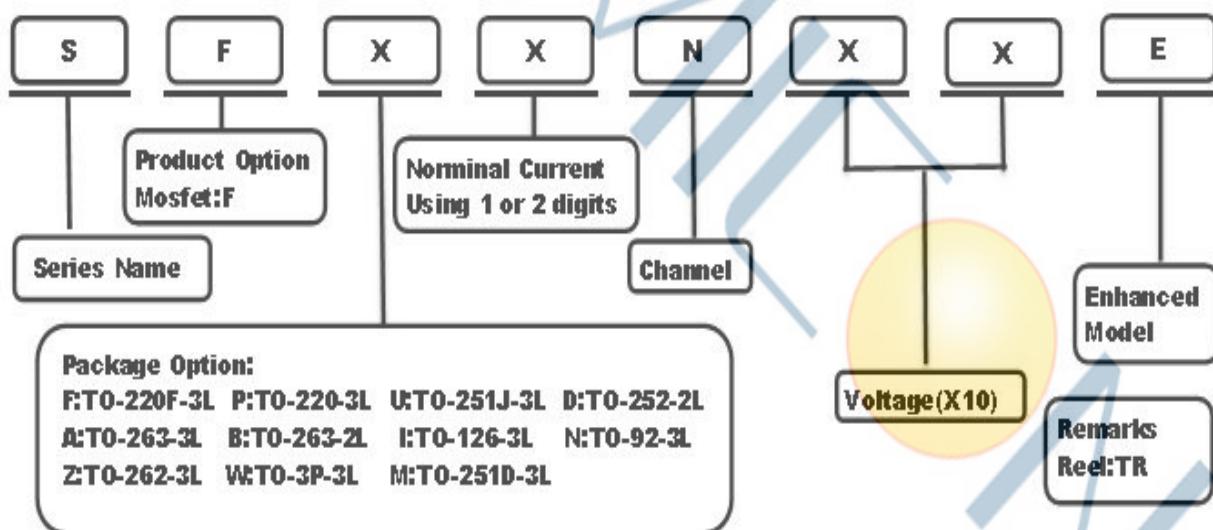
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 59A, 100V, $R_{DS(on)(typ)}=18m\Omega @ V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFP59N10	TO-220-3L	SFP59N10	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current $T_c = 25^\circ\text{C}$	I_D	59	A
$T_c = 100^\circ\text{C}$		40	
Drain Current Pulsed	I_{DM}	230	A
Power Dissipation($T_c=25^\circ\text{C}$) -Derate above 25°C	P_D	200	W
		1.3	$\text{W}/^\circ\text{C}$
Repetitive Avalanche Energy (Note 1)	E_{AR}	20	mJ
Operation Junction Temperature Range	T_J	-55~+150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55~+150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.75	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	V_{BDSS}	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	100	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(\text{on})}$	$V_{GS}=10\text{V}, I_D=28.0\text{A}$	--	18	23	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHZ}$	--	3120	--	pF
Output Capacitance	C_{oss}		--	408	--	
Reverse Transfer Capacitance	C_{rss}		--	73	--	
Turn-on Delay Time	$t_{d(\text{on})}$	$V_{DD}=50\text{V}, I_D=28\text{A}, R_G=25\Omega$	--	12	--	ns
Turn-on Rise Time	t_r		--	60	--	
Turn-off Delay Time	$t_{d(\text{off})}$		--	46	--	
Turn-off Fall Time	t_f		--	47	--	
Total Gate Charge	Q_g		--	130	--	nC
Gate-Source Charge	Q_{gs}	$V_{DS}=80\text{V}, I_D=28\text{A}, V_{GS}=10\text{V}$	--	28	--	
Gate-Drain Charge	Q_{gd}		--	45	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I _S	Integral Reverse p-n Junction Diode in the MOSFET	--	--	59.0	A
Pulsed Source Current	I _{SM}		--	--	230.0	
Diode Forward Voltage	V _{SD}	I _S =28A, V _{GS} =0V	--	--	1.2	V
Reverse Recovery Time	T _{rr}	I _S =28A, V _{GS} =0V,	--	150	--	ns
Reverse Recovery Charge	Q _{rr}	dI _F /dt=100A/μS (Note 2)	--	680	--	μC

Notes:

1. L=0.7mH, I_{AS}=28.0A, V_{GS}=10V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

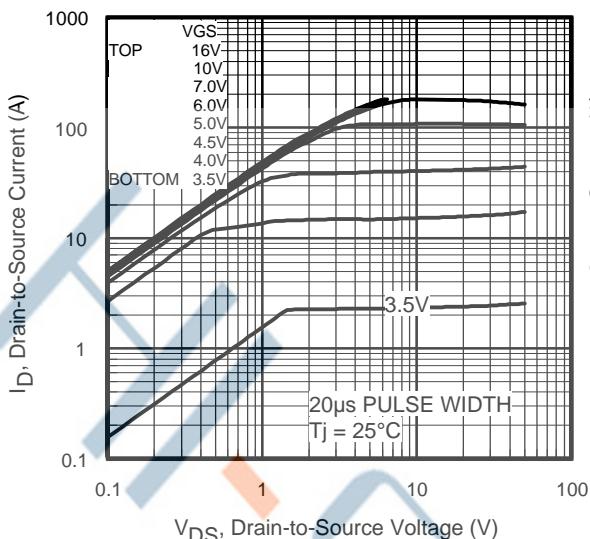


Fig 1. Typical Output Characteristics

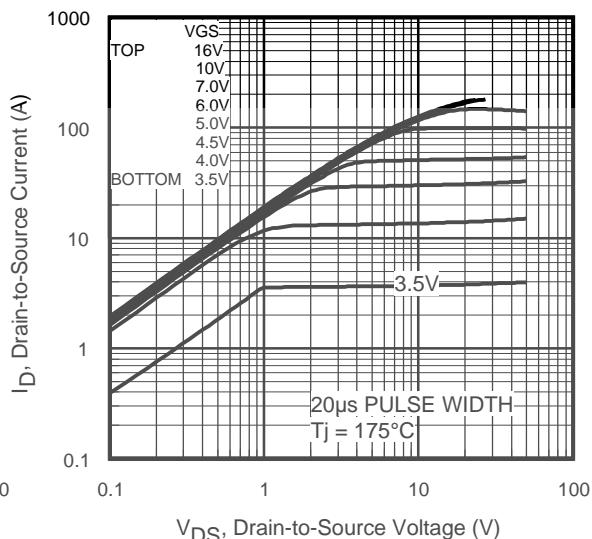


Fig 2. Typical Output Characteristics

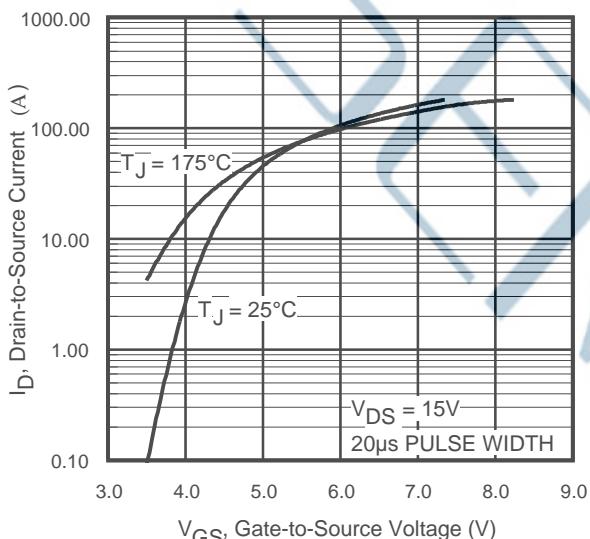


Fig 3. Typical Transfer Characteristics

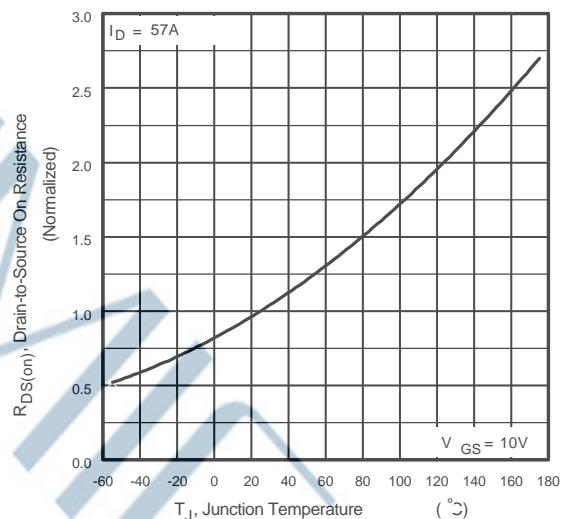


Fig 4. Normalized On-Resistance Vs. Temperature

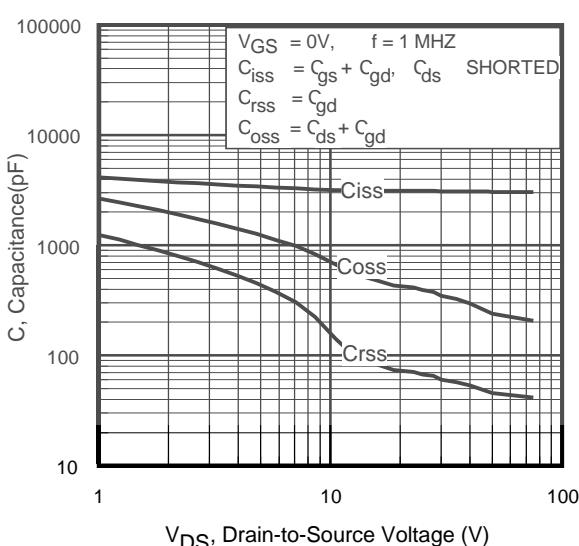


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

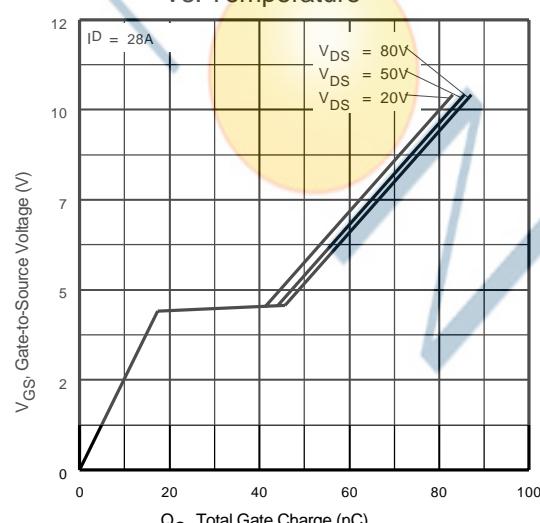


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS (continued)

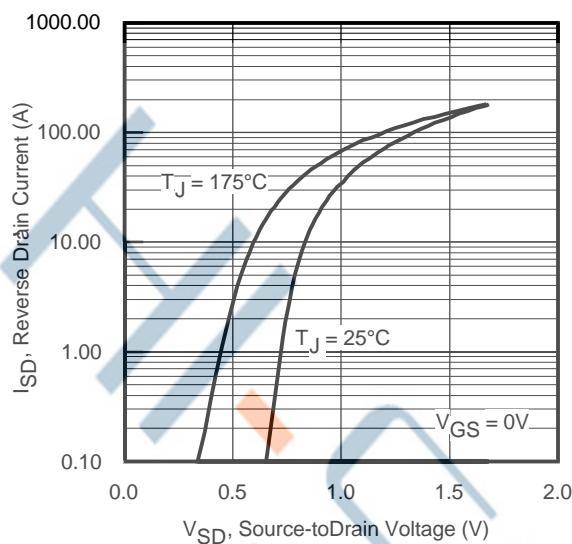


Fig 7. Typical Source-Drain Diode Forward Voltage

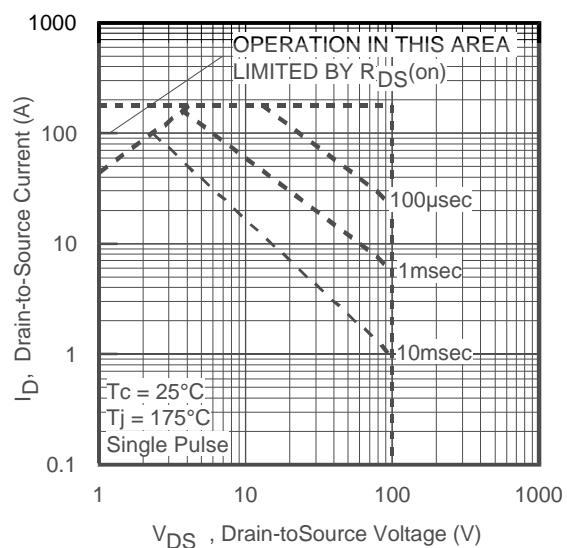


Fig 8. Maximum Safe Operating Area

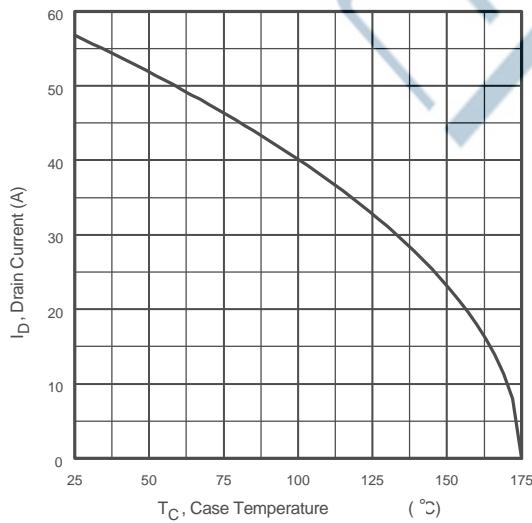
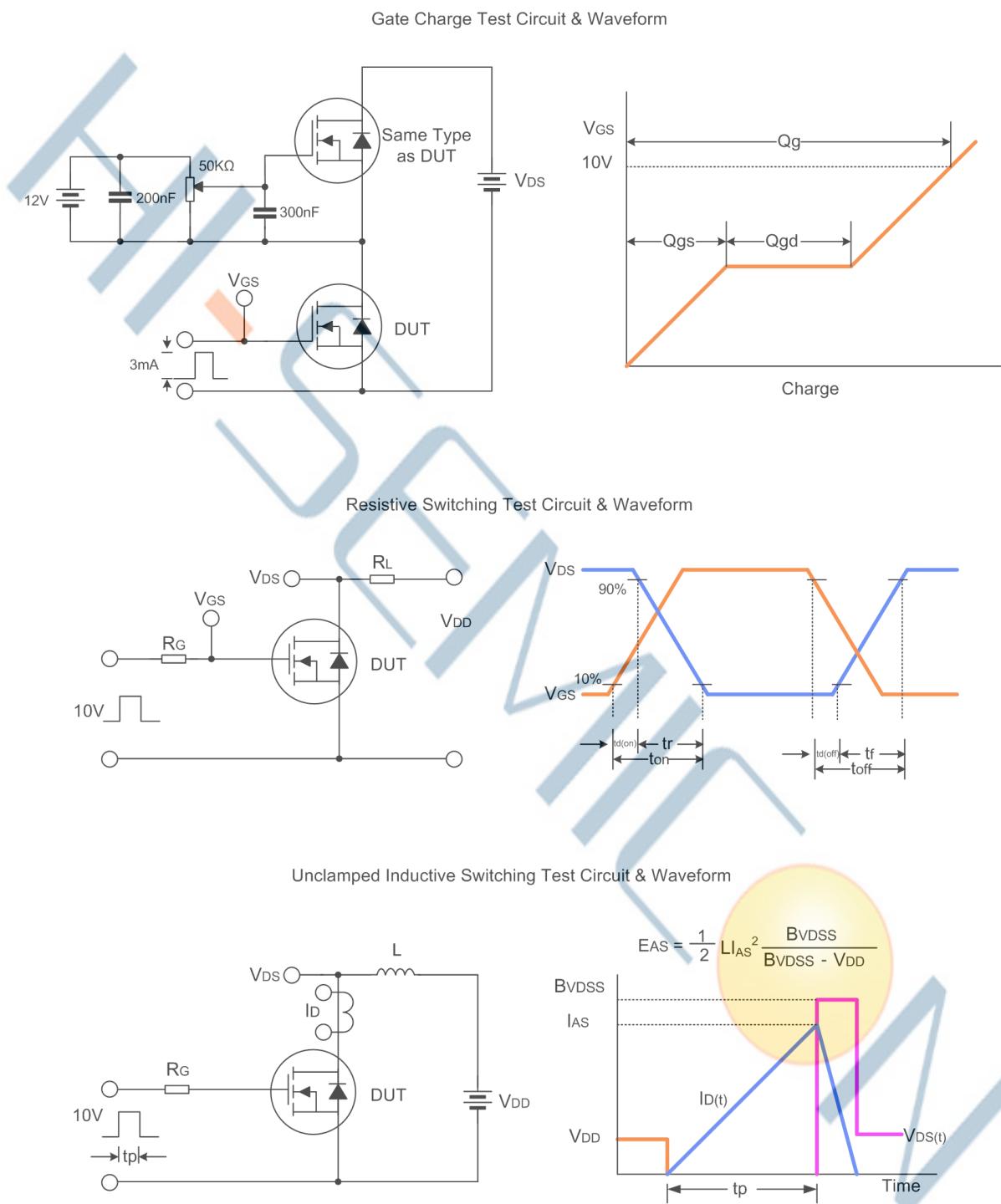


Fig 9. Maximum Drain Current Vs. Case Temperature

TYPICAL TEST CIRCUIT



PACKAGE OUTLINE

